

3D & Chiplet Test Workshop - Advanced Program

Thursday, September 25th

16:00 - 16:10 **Opening Remarks** – Yervant Zorian (Synopsys), General Chair
Saman Adham (TSMC) and Sreejit Chakravarty (Ampere Computing), Program CoChairs

16:10 – 16:50 Keynote Address: (Joint Session)

**From Lifecycle Intelligence to Packaging Innovation:
How SLM and Probe Data Can Unlock Automotive-Grade Advanced ICs**
Davide Appello, Vice President, Product Strategy, Technoprobe (Micro Probe)

16:50 – 17:30 Visionary talk:

UCIe Role in 3DIC and Chiplet Development,
Debendra Das Sharma, Chair, UCIe Consortium (Intel)

17:30 - 18:30 Panel: EDA/IP Solutions for Chiplet Test & Repair

Panelists: Yervant Zorian (Synopsys), Martin Keim (Siemens EDA), Brion Keller (Cadence)

18:30 – 20:00 Workshops Reception

Friday, September 26th

8:00 - 10:00 Session 1: Chiplet Interconnect Repair
Saman Adham (Moderator)

8:00 – 8:30 **Closer-to-Functional Single-Cycle Interconnect Tests**
Irith Pomeranz (Purdue University)

8:30 – 9:00 **CIRA – Chiplet Interconnect Repair Analysis – An Open-Source Tool for Chiplet Repairability Analysis**
Adrian Evans (presenter), Théo Bermond (CEA)

9:00 – 9:30 **A Novel Chiplet Interconnect Test Architecture & Repair Mechanism for Multi-Die System**
Tapan J Chakraborty, Anshuman Chandra, Moiz Khan, Rajesh Pendurkar, Adam Cron, Po-Yao Chung
(PIEEE3405 WG)

9:30 – 10:00 **Trends in Multi-Die Test with high-throughput protocol & non-protocol aware interfaces**
Sri Ganta(Synopsys), Manish Arora (Synopsys), Sandeep Goel (TSMC)

10:00 - 10:30 Coffee Break

10:30 - 12:00 Session 2: HBM and Chiplet Test and Reliability
Tapan Chakraborty (Modertor)

10:30 – 11:00 **HBM KGSD testing strategy**
Shu-Liang Nin (TSMC)

11:00 – 11:30 **Leveraging SLM EXTRAM Methodology for Custom HBM**
Arun Kumar, Yervant Zorian (Synopsys)

11:30 – 12:00 **3D/Chiplet Test Challenges and Direction**
Phil Byrd (Micron Technology)

12:00 - 1:00 Workshop Lunch

1:00 - 2:30 Session 3: Chiplet Interconnect Defects and Fault modelling
Sandeep Goel (Moderator)

1:00 – 1:30 **Manufacturing Defects & Fault Modeling for Die-to-Die Hybrid Bond Interconnects**
Moiz Khan, Anshuman Chandra (Siemens EDA), Jennifer Dworak (Southern Methodist University) ,
Rajesh Pendurkar (Cadence Design Systems), Saurabh Gupta (Nvidia)

1:30 – 2:00 **Ultra-low Leakage Defect Detection in 3DIC Interconnects: A Silicon Case Study**
Ankita Patidar (TSMC)

2:00 – 2:30 **Leveraging ML to Detect Defective Dies in 3DICs**
Jin Yu (Teradyne)

2:30 – 4:00 Session 4: Industry Best Practices in Chiplet Developments
Martin Keim (Moderator)

2:30 – 3:00 **Best Practices for Testing 2.5D Chiplet Package Designs**
Vineet Pancholi (Amkor)

3:00 – 3:30 **Latest Trends in Wafer Test for Chip to Chip Interfaces**
Raajit Lall (FromFactor)

3:30 – 4:00 **Cost Analysis of Sector Symmetry and Cut Method in 3D IC with Heterogeneous Wafer Defect Distribution**
Tanusree Kaibartta, Saksham Jha, Digvijay Anand and Debesh Kumar Das (IITISM Dhanbad)

4:00 – 4:10pm **CLOSING REMARKS**